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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/822,768	03/30/2001	Hajime Washio	55321 CIP (70904)	6956

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EDWARDS & ANGELL, LLP
P.O. BOX 55874
BOSTON, MA 02205

EXAMINER	
ABDULSELAM, ABBAS I	

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 05/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/822,768	WASHIO ET AL.	
	Examiner	Art Unit	
	Abbas I Abdulselam	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-52 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-24, 37 and 39-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murade (USPN 6531996) in view of Kimura (USPN 6281826).

Regarding claims 1 and 16, Murade teaches a liquid crystal device (200) including a TFT array substrate (1) with a plurality of pixel electrodes (11) disposed in a matrix fashion. Murade discloses a plurality of data lines (35), a plurality of scanning lines (31) and a plurality of switching devices such as TFTs (30) as shown in Fig. 1. Murade further teaches a pre-charging circuit (201) for supplying a pre-charging signal having predetermined voltage level to the plurality of data lines (35) before an image signal is supplied. In conjunction to pre-charging circuit (201), Murade teaches a sampling circuit (301) for sampling the image signal and supplying the resultant signal to the plurality of data lines (3). For example, Murade teaches that sampling any of the image signals VID1-VID6 corresponding to data lines (35) in order that the

resultant signals on the corresponding data lines (35) are written (col. 13, lines 35-39). Moreover, Murade teaches a scanning line driving circuit (104) supplying a scanning signal in the form of a pulse in line–sequential fashion to the scanning line (31). Murade further adds that in synchronization with the scanning signal generated by the scanning drive circuit (104), the data line driving circuit (101) generates a sampling circuit driving signal in accordance with a reference clock signal, CLK. See col. 12, lines 43-67 and col. 13, lines 1-50. Murade discloses that the pre-charging circuit (201) and the sampling circuit (301) both operate in an AC mode, whereas driving circuits (101, 104) operate in a DC mode. See col. 16, lines 1-18. Murade teaches the same pre-charging signal NRS is supplied from an external control circuit to two contacts (103a) and (103d) via an external terminal (102) allowing all the TFTs (202) to turn on at the same time without any delay. (col. 13, lines 50-62). Murade further teaches that through use of the external control circuit, it is possible to reduce the difference in contrast between the left and right areas of the screen. See col. 13, lines 65-67.

However, Murade does not teach "a pre-charging circuit for writing a pre-charging voltage inputted in synchronism with a pre-charging control signal into a plurality of data signal lines in a predetermined period of time; and wherein a pre-charging voltage stabilizing section for stabilizing a pre-charging voltage as said to the pre-charging circuit, so as to suppress fluctuation in said pre-charging voltage is provided on a preceding stage of said pre-charging circuit." Kimura on the other hand teaches a method of pre-charging signal lines, whereby the charging/discharging currents of the signal lines may be adjusted by controlling the period of time for which the switches are connected to the signal lines thereby pre-charging the signal lines to a predetermined voltage levels. Kimura teaches a signal line pre-charging circuit (6300) as

shown in Fig. 66 including a switch controller (6320) and pre-charging lines (L1 and L2) held at pre-charging voltages, (Vpca and Vpcb), (as illustrated in Fig. 46) in order that the signal line (S) is pre-charged, so that the voltage on the signal lines (S) periodically varies with a period, T as shown in Fig. 46B. See col. 40, lines 56-64, col. 43, lines 63-67 and col. 44, lines 1-4, Fig. 46 and Fig. 66.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Murade's liquid crystal display system to adapt Kimura's method of pre-charging signal lines as illustrated in Fig. 46 and Fig. 66. One would have been motivated in view of the suggestion in Kimura that a pre-charging circuit (6300) as shown in Fig.66 and demonstrated in Fig. 46 is functionally equivalent to the desired pre-charging circuit as claimed. The use of pre-charging circuit helps achieve a liquid crystal display system a pre-charging accuracy as taught by Kimura.

Furthermore, Kimura teaches that if the equivalent capacitance (stray capacitance, C22, C23) of the pre-charging voltage lines (L1, L2) are sufficiently great compared with equivalent capacitance (stray capacitance, C21) of the signal line (S), then the effects of the capacitance of the signal line can be neglected, and therefore, pre-charging accuracy can be further improved. Kimura teaches that a precise voltage can be applied to the signal lines and thus a high pre-charging accuracy (stability) can be achieved. It would have been obvious the pre-charging accuracy described meets and is equivalent to the desired "pre-charging voltage stabilizing section".

Regarding claims 11, 14, 21 and 37, Murade has been discussed above. In addition, Murade discloses that the pre-charging circuit (201) and the sampling circuit (301) both operate

in an AC mode (col. 16, lines 1-2). Murade also illustrates the use of power supply (1010) as shown in Fig. 16. However, Murade does not teach a pre-charging voltage stabilizing section, which is composed of current controlling means and a charge holding means. Kimura on the other hand teaches that pre-charging can be performed by charging or discharging only the signal lines (or the capacitor C21 in Fig. 46A, which has a charge QA corresponding to a voltage, V1 that is stored according to QA=C21.multidot.V1. See col. 41, 48-53, col. 42, lines 13-24 and Fig. (46A-C). Moreover, Kimura teaches as shown in Fig. 14B, the use of capacitors (2000, 2100) with respect a flow of current "IS" or "IR" occurring depending on the relative a magnitude of VC or VX. See col. 21, lines 21-26. Therefore, it would have been obvious that the charge (QA) storage as shown on Fig. 46, and the flow of current as demonstrated in Fig. 14B satisfy the desired composition of charge holding means and current controlling means.

Furthermore, Kimura teaches the effects of operation of pre-charging signal lines as shown on Fig. (76A-76B) with a signal line "S1", and the liquid crystal cell (6022, 6024) each displaying a "black signal" having black level voltage (B1, B2), during scanning periods (T1, T2) respectively. Kimura further teaches that although "black" is displayed by both cells, the signal voltage applied to these cells are opposite in polarity. See col. 3, lines 52-60. Kimura also discloses curves (R1, R2) over which signal line voltage changes from Black level voltage B1 to black level voltage B2. Moreover, as shown on Fig. 51, Kimura teaches a signal line pre-charging circuit (6300) including the use switches (SW1a, SW1b, SW2a, SW2b) together with scanning line driving circuit (6200). Thus It would have been obvious that from the curves (R1, R2) of Fig. 76A, and from the configuration of switches of Fig. (51), one can deduce the desired step of "suspending a scanning signal line".

Regarding claims 2 and 4, Murade discloses that pixel electrodes (11) are disposed in a matrix fashion such that when plurality gates are disposed in the TFT (30), the TFT has a larger off-resistance, which results in a reduction in leakage current. See col. 22, lines 5-12. Murade also teaches the pre-charging signal NRS is written on all the data lines (35). See col. 18, lines 56-58.

Regarding claim 3, Murade teaches the use of storage capacitors (70) with respect to pixel electrodes (11) See col. 12, lines 61-64 and Fig. 1.

Regarding claim 5, Murade teaches capacitance lines 31' that may be formed in such a manner they extend in a direction parallel to the scanning line (31). Murade also shows that the capacitance lines 31' extend below the scanning lines so that storage capacitance are formed between the scanning lines and the capacitance lines. See col. 12, lines 65-67 and col. 13, lines 1-3.

Regarding claims 6-8, Murade teaches a pre-charging circuit facilitating writing a high quality image signal on the data lines such that the polarity of voltage applied to the data line is inverted at a predetermined frequency in order that a liquid crystal is driven in an AC mode. See col. 1, lines 39-50. Moreover, Murade teaches a pre-charging circuit with respect to polarity inversion. See col. 18, lines 26-49. Murade further teaches reduction of current leakage implemented with respect to TFT (30). See col. 22, lines 5-12.

Regarding claims 9-10, Murade teaches a pre-charging circuit (201) with respect to a scanning line driving circuit (104) operating in a DC mode. See col.16, lines 8-18. Murade

discloses that the liquid crystal layer (50) is prevented from receiving leakage of a DC voltage component. See col. 16, lines 5-15.

Regarding claims 17-20, see Murade's Fig. 1 including pre-charging circuit and capacitor (70, 201), also see Fig. 6 where a time chart associated with pre-charging circuit-driving signals is demonstrated. Murade teaches that the pre-charging circuit (201) operates in an AC mode, and the driving circuits (101, 104) operate in a DC mode. See col. 16, lines1-18.

Regarding claims 22-24, Kimura teaches scanning lines (H1, H2....) driven by a scanning line driving circuit (6200) as shown in Fig. 51, and driving each scanning lines with respect to a period of time from the pre-charging operation to the signal lines driving operation (Fig. 63)

Regarding claims 12-13 and 15, Murade teaches a pre-charging circuit facilitating writing a high quality image signal on the data lines such that the polarity of voltage applied to the data line is inverted at a predetermined frequency in order that a liquid crystal is driven in an AC mode. See col. 1, lines 39-50. Moreover, Murade teaches a pre-charging circuit with respect to polarity inversion. See col. 18, lines 26-49. Murade further teaches reduction of current leakage implemented with respect to TFT (30). See col. 22, lines 5-12.

Regarding claims 39-41, Murade's Fig. 1, where a TFT substrate (1) includes a pre-charging circuit (201), a scanning line driving circuit (104), and a data line driving circuit (101).

Regarding claims 42-43, Murade discloses switching devices of a liquid crystal device each formed into a structure of a coplanar type polysilicon TFT. See col. 26, lines 38-40.

3. Claims 25-36 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murade in view of Kimura and in further view of Takeda et al. (USPN 5223824).

Murade as modified has been discussed above. However, Murade does not teach suspending a scanning signal for a predetermined period of time such that the predetermined period of time is variable. Takeda on the other hand, teaches a quiescent circuit (33), which prevents for particular period the scanning pulses from being generated into row electrode (26). See col. 6, lines 27-41, Fig. 1 and Fig. 3.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Murade's display system to adapt Takeda's quiescent circuit (33). One would have been motivated in view of the suggestion in Takeda that the quiescent circuit (330) equivalently performs suspension of scanning signals for the desired period of time. The use of a quiescent circuit (33) helps function a display system with variable scan lines as taught by Takeda.

4. Claims 44-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murade in view of Kimura, Takeda et al. and in further view of Mori et al. (USPN 5243202).

Murade as modified has been discussed. However, Murade not teach a data signal line driving circuit, a scanning signal line driving circuit and pixels are manufactured at a process temperature of not more than 600 degree centigrade. Mori on the other hand discloses TFTs to be manufactured at nearly constant temperature through a series of steps. Mori teaches manufacturing method of the thin film transistor divided into 9 steps with each step having its corresponding film forming temperature. See col. 11- 12, TABLE 2. For example, Mori shows in step 7 (col. 13, lines 33-40) a SiN film formed as interlayer insulating film (118) that insulates a scanning signal line (104) from the data signal line (105) with the film-from temperature range of 250 to 270 degree centigrade. See col. 8, lines 36-40.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Murade's display system to adapt Mori's method of manufacturing a thin film transistor including film forming temperature as shown in TABLE 2. One would have been motivated in view of the suggestion in Mori that the film forming temperature as indicated in Table 1 provides the desired manufacturing temperature of not more than 600 degree centigrade. The use of a thin film transistor helps function an active matrix display system as taught by Mori et al.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communication from the examiner should be directed to **Abbas Abdulselam** whose telephone number is **(703) 305-8591.** The examiner can normally be reached on Monday through Friday (9:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard Hjerpe**, can be reached at **(703) 305-4709.**

Any response to this action should be mailed to:

Commissioner of patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314

Hand delivered responses should be brought to Crystal Park II, Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology center 2600 customer Service office whose telephone number is (703) 306-0377.

Abbas Abdulselam

Examiner

Art Unit 2674

April 22, 2004

XIAO WU
PRIMARY EXAMINER